BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(END SEMESTER EXAMINATION)

CLASS: BE
BRANCH: ECE/EEE/CS/IT

SEMESTER : III
SESSION : MO/15

SUBJECT: EC3201-DIGITAL ELECTRONICS

TIME: 3 HOURS

FULL MARKS: 60

INSTRUCTIONS:
1. The question paper contains 7 questions each of 12 marks and total 84 marks.
2. Candidates may attempt any 5 questions maximum of 60 marks.
3. The missing data, if any, may be assumed suitably.
4. Before attempting the question paper, be sure that you have got the correct question paper.
5. Tables/Data hand book/Graph paper etc. to be supplied to the candidates in the examination hall.

Q.1(a) Prove the following identity using Boolean algebra and DeMorgan's theorem. [2]
$\overline{AB + BC + CA} = \overline{AB} + \overline{BC} + \overline{CA}$

(b) Implement the function: $F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 8, 9, 10)$ with two levels NOR-OR form. [4]

(c) Using Quine-McCluskey method of tabular reduction, obtain a minimal POS expression for the function: $F(A, B, C, D) = \prod M(1, 4, 5, 11, 12, 14) . d(5, 7, 15)$. [6]

Q.2(a) Explain the realization of a full-adder using two half-adders. [2]

(b) Obtain a 16 x4 line encoder with a dual 8-line to 3-line encoder having separate enable inputs and enable outputs. Use a block diagram construction. [4]

(c) Explain the operation of a 4-bit BCD-adder with correction detection circuit using block diagram construction. [6]

Q.3(a) Develop the characteristic table of SR flip-flop and derive the characteristic equation. [2]

(b) Design a type-D counter that goes through states 0, 2, 4, 6, 0----. Is the counter self-starting? [4]

(c) Explain the operation of a 3-bit asynchronous down counter using JK flip-flops. Also implement the truth table and timing diagram. [6]

Q.4(a) What is state table? What does each row, column and entry of the state table represent? [2]

(b) A sequential circuit with two T flip-flops 'A' and 'B'; one input-X and one output-Y, is described by flip-flop input functions and circuit output function as: $T_A = B \oplus X$, $T_B = (AB + \overline{B}X + A\overline{X})$ and $Y = (A\overline{X} + \overline{A}\,\overline{B}\,X)$. Derive the state table and state diagram for the circuit. [4]

(c) Design a clocked sequential circuit using JK flip-flop for the state diagram shown in Figure-1. Use state reduction and binary state assignment. [6]

Q.5(a) What happens if an input of TTL gate is left floating? [2]

(b) Implement the function: $F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 8, 9, 12)$ using CMOS logic. [4]

(c) Explain how the diode-D in active pull-up circuit keeps the pull-up transistor in cut-off when the output is in LOW-state, in TTL NAND gate. [6]

Q.6(a) What is a non-saturated binary? What is its advantage? [2]

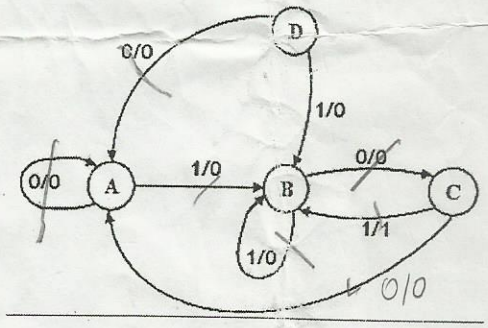
(b) Find the period of output and the frequency of oscillation of an collector coupled astablemultivibrator with $R_1 = R_2 = 25\ K\Omega$ and $C_1 = C_2 = 0.2\ \mu F$. [4]

(c) Explain the operation of a monostablemultivibrator circuit using operational amplifier with suitable waveforms. Obtain the expression for the output pulse width. [6]

Q.7(a) Distinguish between dynamic and static memory. [2]

(b) Implement the block diagram of 4K x 32 RAM using series connected 1K x 32 RAM memory chips. [4]

(c) Implement the combinational circuit defined by the functions: $F_1(A, B, C, D) = (A\overline{C} + B\overline{C}D)$, $F_2(A, B, C, D) = (AB\overline{C} + \overline{B}C + \overline{A}\overline{C}Z)$ by a suitable PROM with truth table. [6]



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