(Please write your Exam Roll No.) Exam Roll No. 0321590411

END TERM EXAMINATION

FIRST SEMESTER [MCA] DECEMBER 2011

Paper Code: MCA 107 **Subject: Computer Organization**

Time : 3 Hours **Maximum Marks :60**

Note: Q.No. 1 is compulsory. Attempt any question from each unit.

Q1. Answer the following: **(2x10=20)**

(a) Why data bus is bidirectional and address bus is unidirectional in most microprocessors?

(b) What is non-maskable Interrupts?

(c) What is race around condition?

(d) Subtract -24 from 21 in 2's complement format.

(e) Define pipeline speedup and throughput.

(f) Determine the reverse polise nation for A/(B+C)

(g) What is software pipelining?

(h) What happens when an RET instruction at the end of a subroutine is executed?

(i) What is meant by a dedicated computer?

(j) Which instructions limit the RISC architecture?

Unit-I

Q2. (a) Desing multiplexer implementations for the following functions using the numerical method. The simulation should be used to check the workings. **(5)**

$Z=f(A,B,C,D) = \Sigma (0, 1,2,3,5,7,8,10,12,13,15)$.

(b) Explain the working mechanism of edge triggered and level triggered Flip-Flops. **(5)**

Q3. (a) Discuss about various microoperations. **(7)**

(b) Discuss master slave Filp-Flop. **(3)**

Unit-II

Q4. (a) Explain multiple bus organizational in detail. **(3)**

(b) What is a stack? Illustrate the use of stack in subroutine processing with suitable diagram. **(7)**

Q5. (a) Discuss the different addressing modes. **(6)**

(b) State the differences between hardwired and micro programmed control unit. **(4)**

Unit-III

Q6. (a) Explain how the performance of the instruction pipeline can be improved. **(5)**

(b) Multiply 111010 with 110011 using Booth's algorithm. **(5)**

Q7. (a) A four segment pipeline implements a function and has the following delays for each segment: **(6)**

(b= 2)

Segment	# Maximum delay
1	17
2	15
3	19
4	14

Where c =2ns,

P.T.O.

(i) What is the cycle time that maximizes performances without allocating multiple cycles to a segment?

(ii) What is the total time to execute the function through all stages?

(b) (i) Why does DMA have priority over the CPU when both request a memory transfer? (2)

(ii) What is the importance of an I/O interface? (2)

Unit-IV

Q8. (a) Consider the design of a three-level memory hierarchy with the following specifications: (6)

Memory Level	Access Time
Cache	t_1=20 ns
Main Memory	t_2 =?
Secondary Memory	t_1=2ms

The design goal is to achieve an effective memory-access time t= 800ns with a cache hit ratio h_1=0.97 and a hit ratio h_2=0.99 in main memory. Find the main memory access time.

(b) State the merits and demerits of associative memory. (4)

Q9. (a) What is virtual memory? Explain how the logical address is translated into physical address in the virtual memory system with a neat diagram. (5)

(b) A digital computer has a memory unit of K x16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the cache accommodate? (5)

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